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X-ray Flat Panel Sensor

C7942 & C7943

User's Guide

Be sure to read the operation manual carefully before the product is used.
If operated differently from the standard procedure in the manual,
a serious accident may occur.
Keep this manual for future reference.

DWG.NO. KR1 – I50001

First Issued Oct. 26, 2000

FormKXX-3513

Table of Contents

Chapter 1 Safety and Handling

- Do not subject the panel sensor module to strong vibrations or shock (such as by dropping the unit).
- The surface of FSP (Flipped Scintillator Plate) can be easily damaged. Do not put any sharp or hard objects on the top of the exposed FSP. Avoid removing the top cover and exposing the sensor.
- Do not bring any liquids into the case of the panel sensor module.
- Clean dust only using an air blower.

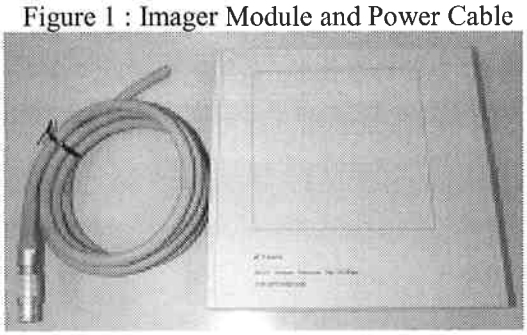
Chapter 2 Introduction

This manual contains a description, installation, operation instructions and other information for the Hamamatus X-ray Flat Panel Image Sensor, C7942 and C7943. Chapter 3 provides a description of the system and Chapter 4 lists the system specifications. Chapter 5 describes the individual components of the imager module. Chapter 6 covers the installation and startup of the system, and Chapter 7 describes the operation of the system.

Chapter 3 Description

Flat Panel Sensor is high speed and high quality imaging module. The unit is designed for x-ray imaging for use in medical imaging, non-destructive testing (NDT), biomedical and other applications.

Figure 1 : Imager Module and Power Cable



C7942 and C7943 includes the following:

- Imager Module
- Cable for power supply connection (Gray cable)

Chapter 4 System Specifications

Functional Specifications

Items	C7942	C7943
Readout	Charge amplifier array	
Video output	RS422 (differential) 12 bit	
Output data rate	15.15 MHz	
Synchronous signal	RS422 (differential)	
bin0, 1, ExtTrg, IntExt	TTL	

Absolute Maximum Ratings (Ta=25degC)

Items	Symbols	Ratings	Units
Supply voltage for digital circuitry (+5V)	D.vdd	+ 6.0	V
Supply voltage for analog circuitry (+5V)	A.vdd	+6.0	V
Supply voltage for analog circuitry(+/-7.5V)	V(+/-7.5)	+/-12	V
Operating Temperature (not condensed)	Topr	-0 to +35	deg
Storage Temperature (not condensed)	Tstg	-0 to +50	deg

Electrical specifications A.vdd=5.0V, D.vdd=5.0V, V(+/-7.5)=+/-7.5V, 25degC

Items	Symbols	C7942 (Typ.)	C7943 (Typ.)	Units
Pixel size		50	100	um
PD array area		120	124.8	mm
Array number		5.76	1.56	M pixels
Frame speed (single operation)	Sf(int)	2	7	Frame / s
Frame speed (2x2 binning)		4	15	Frame / s
Frame speed (4x4 binning)		9	30	Frame / s
Frame speed external(single operation)	Sf(ext)	Sf(int) to 0.1	Sf(int) to 0.1	Frame / s
Noise (rms.)	N(rms.)	1100	2300	Electrons
Saturation Charge	Csat	2.2	10	M electrons
Resolution	Reso	8	5	Line pairs / mm
D range		2000	4300	-
Number of elements	-	2400 x 2400	1248 x 1248	Pixels
Effective elements		2240 x 2368	1216 x 1232	Pixels
Defect line *		20 Max.	10 Max.	lines
Scintillator	-	CsI		-

* Without a couple of adjacent defect line that has no response.

Physical Dimensions

The top cover is made of Aluminum 1.0 mm thickness.
This top cover plate is not solid enough against the mechanical stress. Please take care on the operation and handling.

Figure 2-1 : C7942 Physical Dimensions (unit : mm)

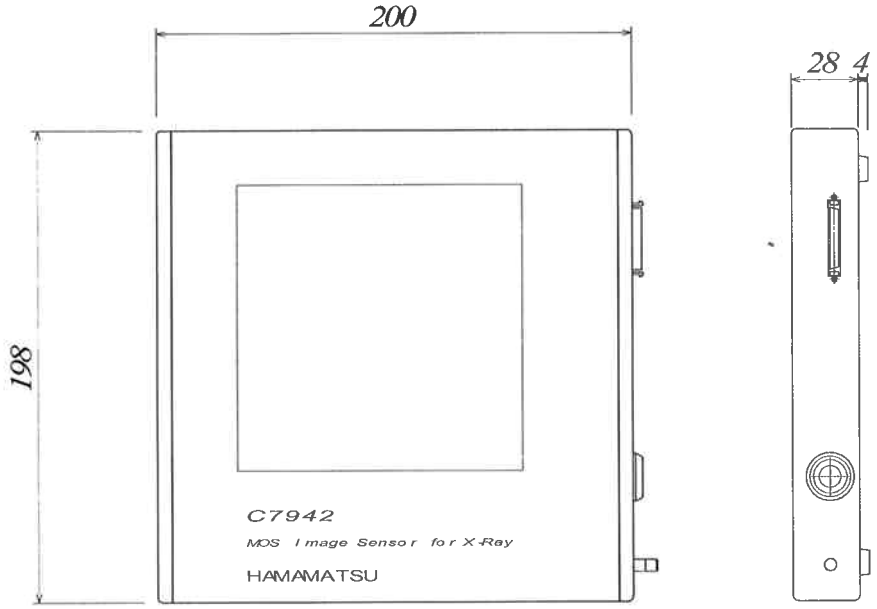


Figure 2-2 : C7943 Physical Dimensions (unit : mm)

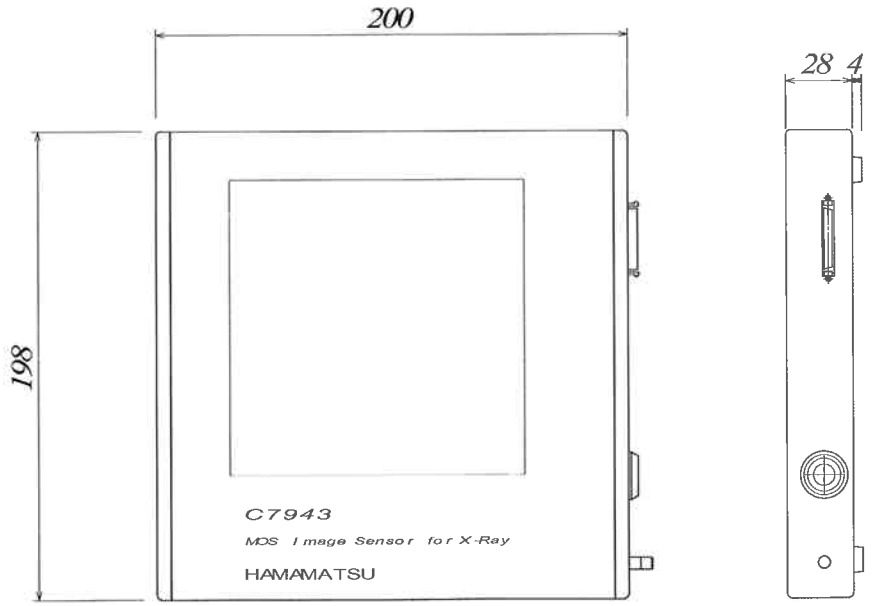
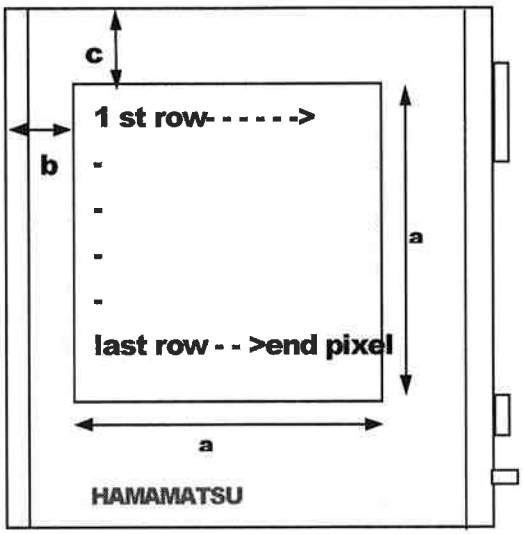
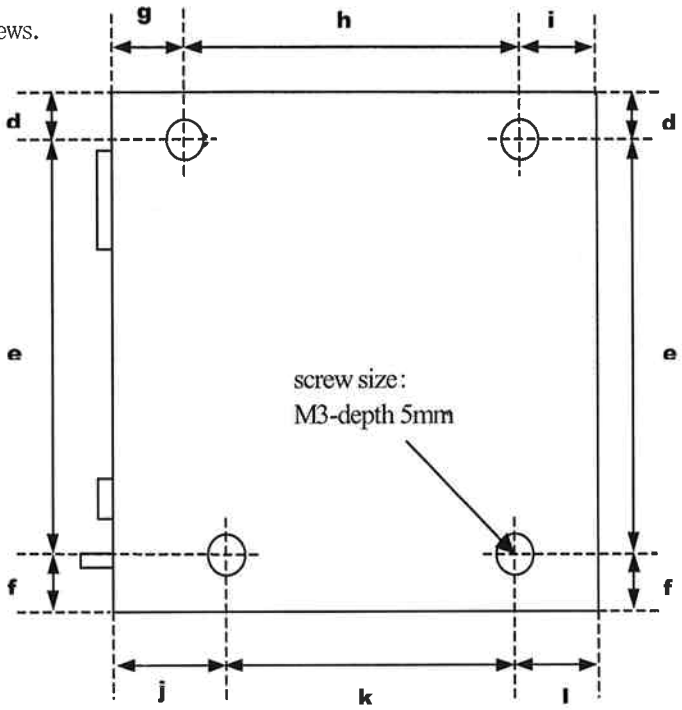


Figure 2-3 : The position of photodiode matrix and female screws.

The position of photodiode matrix and female screws.





The origin is on the corner of "b" and "c".

	C7921	C7942	C7943	(mm)
a	52.8	120	124.8	
b	33	33	31	
c	33	23	21	
d	11	17		
e	118	165		
f	13	16		
g	17	23		
h	108	150		
I	17	27		
j	17	40		
k	96	127		
l	29	33		

Remove screws inside a black leg and use the screws to fix a flatpanel.

Chapter 5 Components Description

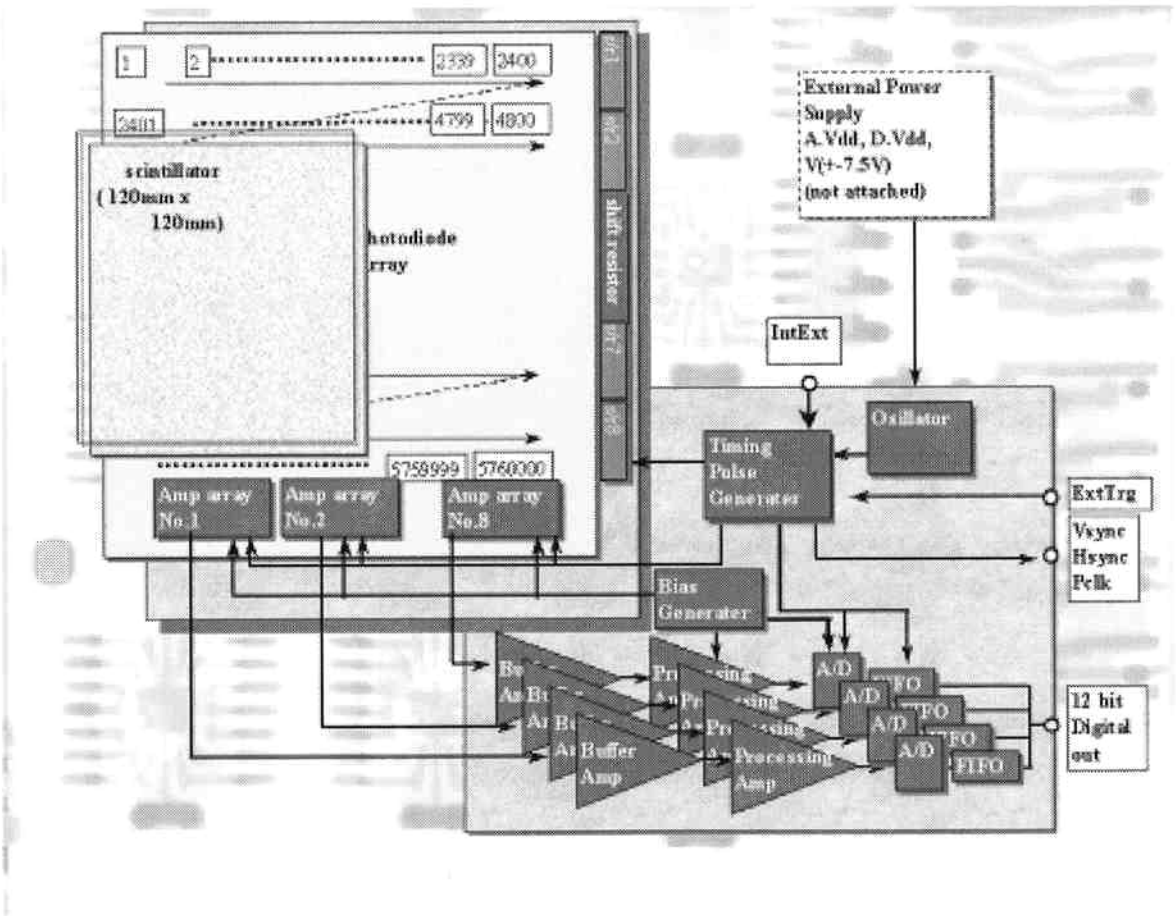
Imager Module

The imager module consists of the MOS photodiode array, a FSP (Flipped Scintillator Plate), shift register, amplifier array and extended electrical circuit board, packaged inside a case made of ferrum.

The internal block diagram of C7942 and C7943 is shown in Figure 3.

X-rays absorbed in the FSP cause light emission directed to the sensor array. The charge created by this illumination is stored in the sensor capacitor until it is read out. The charge is transferred to the corresponding data line by applying a voltage to the MOS gate. Each column of sensor is addressed in sequence from a shift register on the sensor chip. Charge sensitive amplifier on the same chip sense the charge on each of the data lines.

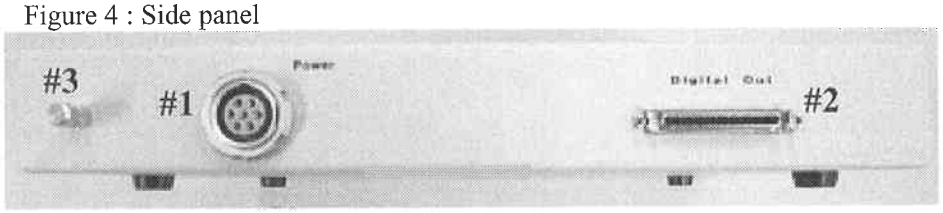
Figure 3 : Block Diagram



Imager side panel

- **Power Input (Figure 4. Receptacle #1)**
  7 contacts receptacle should be connected to the power supply. The power supply cable is attached to this imager module. Details of this cable assignment are described in Chapter 6. The type number of this receptacle is ECG.2B.307.CLV.
  This receptacle is provided by LEMO S.A. (http://www.lemo.ch).
- **Digital Video Out (Figure 4. Receptacle #2)**
  36 contacts receptacle outputs the digital video signal and the synchronization signals for a digital frame grabber board. This receptacle also have I/O port, by using this port, user can change binning setting, trigger setting and integration period easily. Detailed information for these interface signals is described in Chapter 7. The digital video cable is not attached to this imager module. User can choose a suitable cable for each digital frame grabber as an option part for Flat Panel Sensor. Please refer to the 'Flat Panel Sensor Data Sheet.'
- **Earth terminal (Figure 4. Receptacle #3)**
  This earth terminal is connected to the frame grand of the module. It is also connected to analog grand and digital grand in the module.

Figure 4 : Side panel



Chapter 6 Installation and Startup

Shipment contents

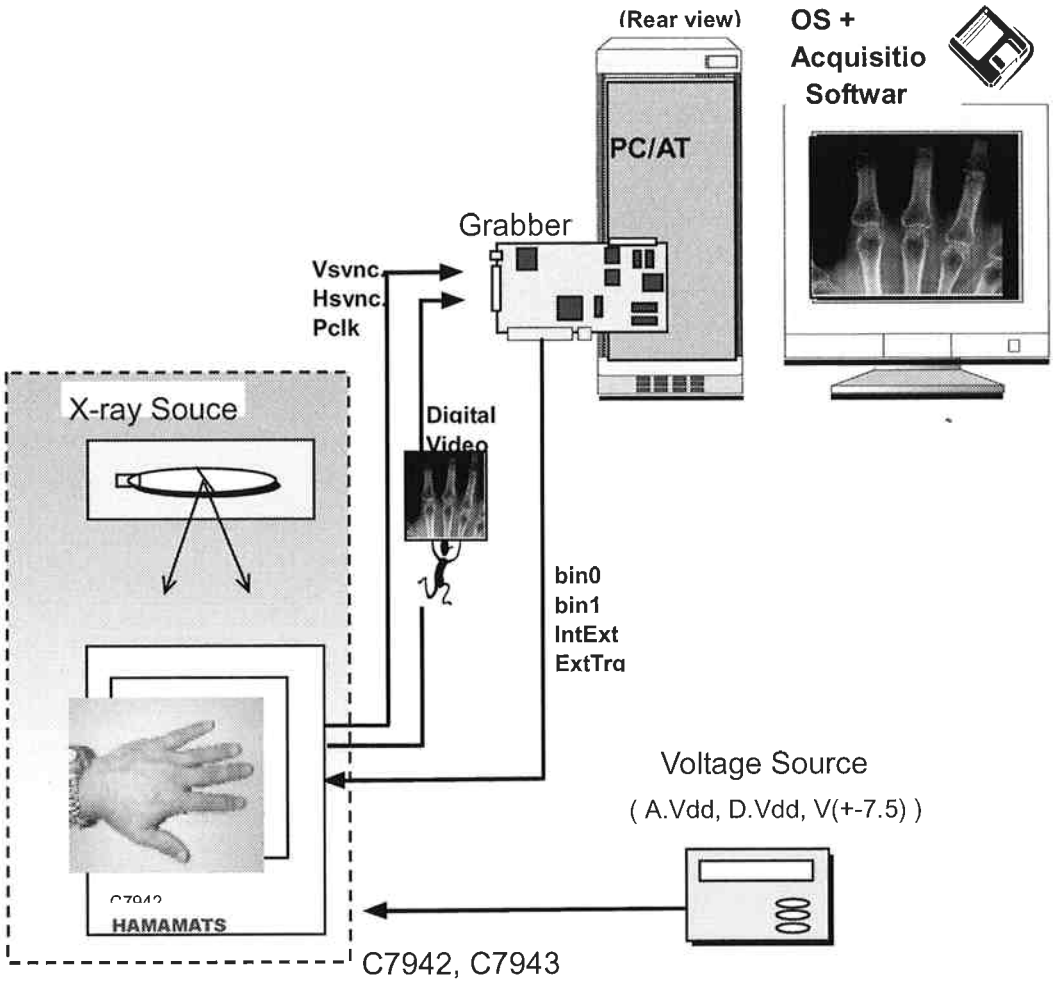
Check the contents to verify that all the items of the imaging system have been included. Contact the factory if anything is missing or damaged.
The contents are following: (Refer to Figure 1.)

1. C7942 and C7943 Imager Module
2. Cable for power supply connection (Gray cable, 2.0m)
3. User's Guide (this paper)

Imaging system construction

For acquiring the x-ray images, C7942 and C7943 should be connected to a power source and a digital frame grabber board installed in a personal computer. Both of the power source and the digital frame grabber are not included in C7942 and C7943 imager modules. An example of the imaging system construction is shown in figure 5.

Figure 5 : System construction example



Personal Computer

Though C7942 and C7943 have over million pixels, they work at very high frame rate. To utilize the full performance of Flat Panel Sensor, high-grade personal computer and frame grabber are required. See the specification of your frame grabber and its requirement.

Cables

- **Cable for power supply connection (Gray cable)**
  7 contacts plug with single key (FGG.2B.307.CLAD92Z) is assembled at the module side of this cable. As another side is bared, user can assemble a suitable plug for general power source. The cable assignment is shown in Table 1.

Above plug is provided by LEMO S.A. (http://www.lemo.ch).

Incorrect connection may result in permanent damage to C7942 and C7943 imager module. Please be careful about the cable assignment.

Table 2. Power source cable assignmer

Cable color : Gray		
	Color	Power Source
1	Brown	+7.5V
2	Red	Analog Gnd
3	Orange	-7.5V
4	Yellow	Analog Gnd
5	Green	Analog +5V
6	Blue	Digital Gnd
7	Purple	Digital +5V
Shield		Analog Gnd

Frame grabber

General-purpose digital frame grabber can be used for acquiring images from C7942 and C7943 imager module.
For the digital video signals and synchronous signals, RS-422 interface is required.
The pin assignment of 36-pin receptacle on the side panel is shown in table 2. As the option cable for the digital frame grabber interface, A8406-01, 06, 07, 08, 02, 03, 04 and 05 are prepared. For more information, please refer to the Flat Panel Sensor Data Sheet.

Table 2. Pin assignment of 36 pin receptacle

Pin No.	Signal	Pin No.	Signal
1	Data1+(MSB)	19	Data1-(MSB)
2	Data2+	20	Data2-
3	Data3+	21	Data3-
4	Data4+	22	Data4-
5	Data5+	23	Data5-
6	Data6+	24	Data6-
7	Data7+	25	Data7-
8	Data8+	26	Data8-
9	Data9+	27	Data9-
10	Data10+	28	Data10-
11	Data11+	29	Data11-
12	Data12+(LSB)	30	Data12-(LSB)
13	bin0 (TTL)	31	Gnd
14	bin1 (TTL)	32	Gnd
15	ExtTrg (TTL)	33	IntExt (TTL)
16	Vsync+	34	Vsync-
17	Hsync+	35	Hsync-
18	Pclk+	36	Pclk-

Unless otherwise specified, signal level is RS422

Power sources

C7942 and C7943 imager module requires 3 types of power source, which are analog +5V, digital +5V and +/-7.5V. Each maximum rated current is shown in Table 3. The voltage margin of A.vdd and D.vdd is from 4.90V to 5.10 V, also from +/-7.0 to +/-8.0V for V(+/-7.5) . The series power source (not switching power source) is recommended for every power.

Table 3. Maximum rated current

	Maximum rated current(mA)
+7.5V	100
-7.5V	-100
A.+5V	700
D.+5V	1000

The separation of analog +5V source and digital +5V source is strongly recommended. The voltages described above are specified at the flat pane sensor side. The impedance of the power cable attached with the flat panel sensor is low enough but it causes 0.1 volt drop. Therefore the voltage at the power source side should be se 0.1 volt higher than the voltage specified above.

Chapter 7 Operation

Timing diagram

The timing diagrams for internal trigger mode and external trigger mode are shown in figure 7 and 8. These information helps the description of the camera parameter file for the frame grabber board (see your grabber's manual).

External trigger signal

Under the internal trigger mode, video signal and synchronous signals always flow out from C7942 and C7943 at the frame speed of Sf(int) which is described in the electrical specification. On the other hand, under the external trigger mode, the external trigger signal is required when the frame grabber starts to readout the image data from C7942 and C7943. The period of this external trigger signal is equal to the period of the integration time. User can set this integration period by using I/O port, #15 pin of the 36-pin receptacle. The sensor starts to forward the video data to the frame grabber board at the rising edge of this signal. The range of this period is restricted between Sf(int) and 0.1 frame/sec, and the duty of this trigger signal should be settled between 1% and 99%(50% is recommended). The voltage of this signal should be compatible with TTL-level. When user selects internal mode, the signal of 'IntExt', #33 pin of the 36-pin receptacle should be set to Low. If #33 pin is set to High, C7942 and C7943 works as the external trigger mode.

Under the external mode, the first image, which follows the first external trigger signal, is usually bright and useless, because the integration period for the first image is usually very long and it's not defined. Therefore, adopting the second image or later one is recommended. (Refer to Fig.7 External Trigger Mode)

Binning Mode

C7942 and C7943 have 1x1, 2x2 and 4x4 binning mode. User can change this binning mode setting by using the I/O port. The pin numbers of 36-pin receptacle for the binning mode select are #13 and #14. Table 4. shows the state of this setting.

Table 4. State of the binning mode setting

	#13 'bin0'	#14 'bin1'
1x1	Low	Low
2x2	High	Low
4x4	High	High

FSP (Flipped scintillator plate)

The Flipped Scintillator Plate is one of the key components of Flat Panel Sensor. It is placed facing onto the high sensitive MOS area image sensor. In case of the x-ray digital imaging with the indirect detection method, the detector requires a scintillator because it does not have a function converting the absorbed x-ray to the electrical signals directly. The FSP absorbs x-ray and converts the energy to visible light for the detector. The base plate is made from a material, which has very low absorption of x-ray because x-ray comes into the scintillator layer through

the base plate.

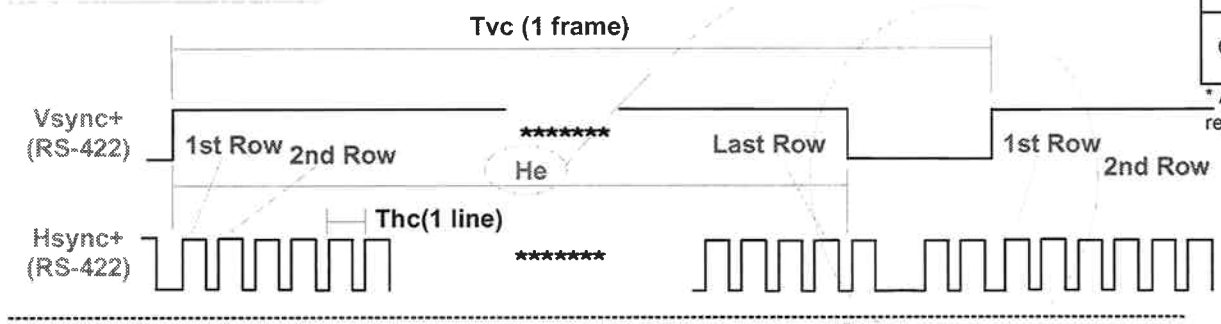
Long term irradiation may result in decreased luminance of the FSP. According to our irradiation experiment, the luminance decreased to 70% after $1x10^6$R irradiation, 35R/min., 80kVp with none aluminum filtration. Decreasing the dose rate, aluminum filtration and intermittent irradiation saves that decrement.

Fig.7

C7942,C7943 MOS Image Sensor for X-ray Rev.2.1 Nov., 2001

Timing Diagram for Camera File

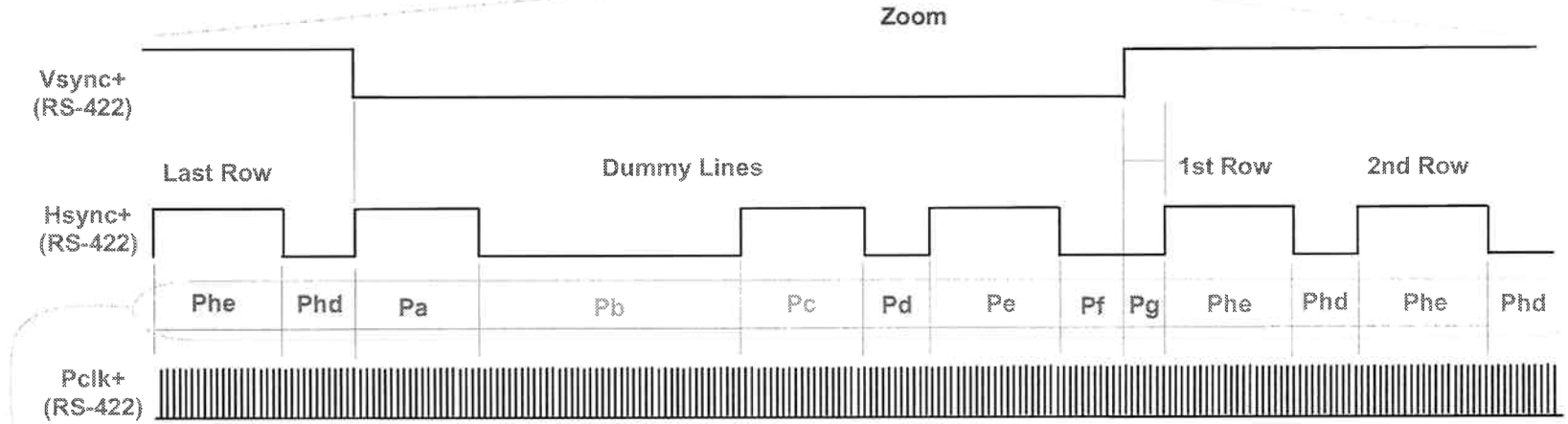
Internal Trigger Mode



Unit : pulses

		He		
		Dummy	Effective	Dummy
C7942	1x1	0	2368	32
	2x2	0	1184	16
	4x4	0	592	8
C7943	1x1	0	1232	16
	2x2	0	616	8
	4x4	0	308	4

* All above pulses are counted at the 'High' region of the Hsync+.



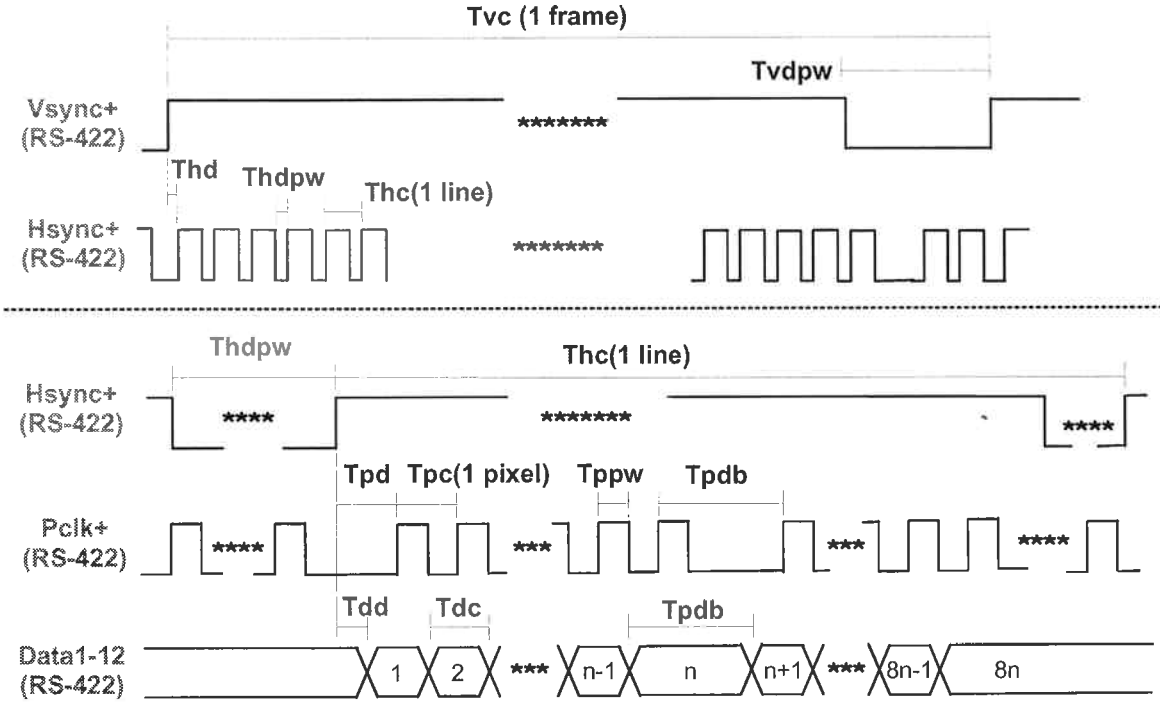
Unit : pulses

		Phe			Phd	Pa	Pb	Pc	Pd	Pe	Pf	Pg
		Dummy	Effective	Dummy	Dummy							
C7942	1x1	0	2240	161	526	2401	3456	2400	541	2400	515	21
	2x2	0	1120	81	1726	1201	4656	1200	1741	1200	1715	21
	4x4	0	560	41	2326	601	5256	600	2341	600	2315	21
C7943	1x1	0	1216	33	334	1249	1920	1248	349	1248	317	27
	2x2	0	608	17	958	625	2544	624	973	624	941	27
	4x4	0	304	9	1270	313	2856	312	1285	312	1253	27

* All above pulses are counted at the rising edge of the Pclk+
* The effective video output is only included in the 'Phe' region. The 'Phe' region is composed with effective pixel clocks and dummy pixel clocks. There is no dummy pixel clock at the top of the 'Phe' region. Therefore the 'Phe' region starts with effective pixel clocks, and dummy pixel clocks follow them as the description of left table.

Fig.8 Timing Diagram for C7942 and C7943

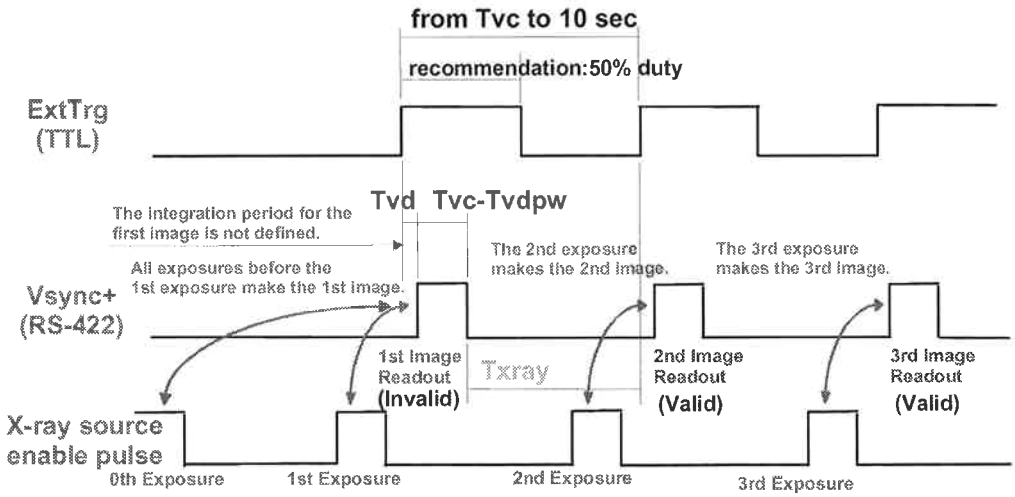
Internal Trigger Mode



In case of C7942, the number of n is 300.
In case of C7943 the number of n is 156.

External Trigger Mode

Hsync+, Pclk and Data1-12 are same as above Internal Trigger Mode.



Txray : Pulse x-ray source should be turned on in this period.

C7942 1x1 Mode

Parameter		Symbol	Typ.	Unit
Vsync	Delay Time (only External Trigger Mode	Tvd	390	us
	Cycle Time	Tvc	470	ms
	Dummy Pulse Width	Tvdpw	770	us
Hsync	Delay Time	Thd	1.4	us
	Cycle Time	Thc	190	us
	Dummy Pulse Width	Thdpw	35	us
Pclk	Delay Time	Tpd	65	ns
	Cycle Time	Tpc	66	ns
	Pulse Width	Tppw	33	ns
	Delay Time Between Each Block	Tpdb	200	ns
Data1-12	Delay Time	Tdd	34	ns
	Cycle Time	Tdc	66	ns

C7942 2x2 Mode

Parameter		Symbol	Typ.	Unit
Vsync	Delay Time (only External Trigger Mode	Tvd	390	us
	Cycle Time	Tvc	230	ms
	Dummy Pulse Width	Tvdpw	770	us
Hsync	Delay Time	Thd	1.4	us
	Cycle Time	Thc	190	us
	Dummy Pulse Width	Thdpw	110	us
Pclk	Delay Time	Tpd	65	ns
	Cycle Time	Tpc	66	ns
	Pulse Width	Tppw	33	ns
	Delay Time Between Each Block	Tpdb	200	ns
Data1-12	Delay Time	Tdd	34	ns
	Cycle Time	Tdc	66	ns

C7942 4x4 Mode

Parameter		Symbol	Typ.	Unit
Vsync	Delay Time (only External Trigger Mode	Tvd	390	us
	Cycle Time	Tvc	117	ms
	Dummy Pulse Width	Tvdpw	770	us
Hsync	Delay Time	Thd	1.4	us
	Cycle Time	Thc	190	us
	Dummy Pulse Width	Thdpw	150	us
Pclk	Delay Time	Tpd	65	ns
	Cycle Time	Tpc	66	ns
	Pulse Width	Tppw	33	ns
	Delay Time Between Each Block	Tpdb	200	ns
Data1-12	Delay Time	Tdd	34	ns
	Cycle Time	Tdc	66	ns

* The number of significant figures is two.

C7943 1x1 Mode

Parameter		Symbol	Typ.	Unit
Vsync	Delay Time (only External Trigger Mode	Tvd	210	us
	Cycle Time	Tvc	130	ms
	Dummy Pulse Width	Tvdpw	420	us
Hsync	Delay Time	Thd	1.8	us
	Cycle Time	Thc	110	us
	Dummy Pulse Width	Thdpw	22	us
Pclk	Delay Time	Tpd	65	ns
	Cycle Time	Tpc	66	ns
	Pulse Width	Tppw	33	ns
	Delay Time Between Each Block	Tpdb	200	ns
Data1-12	Delay Time	Tdd	33	ns
	Cycle Time	Tdc	66	ns

C7943 2x2 Mode

Parameter		Symbol	Typ.	Unit
Vsync	Delay Time (only External Trigger Mode	Tvd	210	us
	Cycle Time	Tvc	66	ms
	Dummy Pulse Width	Tvdpw	420	us
Hsync	Delay Time	Thd	1.8	us
	Cycle Time	Thc	110	us
	Dummy Pulse Width	Thdpw	63	us
Pclk	Delay Time	Tpd	65	ns
	Cycle Time	Tpc	66	ns
	Pulse Width	Tppw	33	ns
	Delay Time Between Each Block	Tpdb	200	ns
Data1-12	Delay Time	Tdd	33	ns
	Cycle Time	Tdc	66	ns

C7943 4x4 Mode

Parameter		Symbol	Typ.	Unit
Vsync	Delay Time (only External Trigger Mode	Tvd	210	us
	Cycle Time	Tvc	33	ms
	Dummy Pulse Width	Tvdpw	420	us
Hsync	Delay Time	Thd	1.8	us
	Cycle Time	Thc	110	us
	Dummy Pulse Width	Thdpw	84	us
Pclk	Delay Time	Tpd	65	ns
	Cycle Time	Tpc	66	ns
	Pulse Width	Tppw	33	ns
	Delay Time Between Each Block	Tpdb	200	ns
Data1-12	Delay Time	Tdd	33	ns
	Cycle Time	Tdc	66	ns

* The number of significant figures is two.

Chapter 8 Warranty

This product is warranted to the original purchaser for a period of 12 months following the date of shipment. The warranty is limited to replacement or repair of any defective material due to defects in workmanship or materials used in manufacture. It does not cover loss or damage of the product due to natural calamity, misuse or total radiation dose over 1 million Roentgen (80kV) even within the warranty period.

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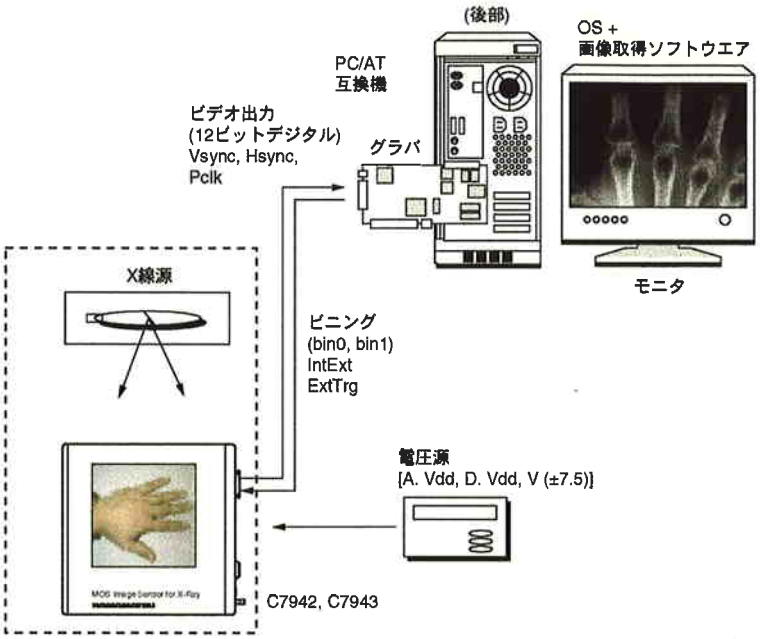
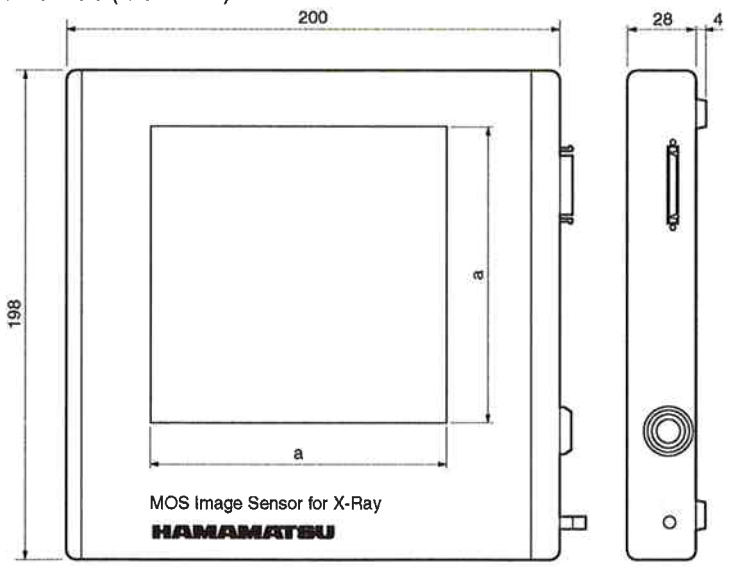
■ 接続

製造元のマニュアルに従って、デジタルフレームグラバボードをパソコンに取り付けてください。I/O コントロールをもった汎用のグラバボードを使用すると、I/O ラインを通して bin0, bin1, intExt, ExtTrg のトリガまたはビニング動作をコントロールできます



KACCC0140JA

■ 外形寸法図 (単位: mm)



上面カバーはアルミ製 (厚さ1.0 mm)

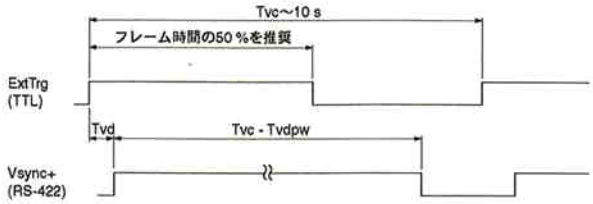
	C7942	C7943
a	120	124.8

KACCA0095JA

■ 使用上の注意

本製品に強い振動や衝撃を与えないように注意してください。(落下などによる強い衝撃を与えると本製品に回復不可能なダメージを与えることがあります。)
X 線に対する必要な安全策や遮蔽は、ユーザの責任よって実施してください。

外部モード



Hsync+, PclkおよびData 1-12は内部トリガモードと同じです。

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C7942

1 × 1 モード (Typ.)

項目		記号	定格値	単位
Vsync	遅延時間 (外部トリガモードのみ)	Tvd	390	μs
	サイクル時間	Tvc	470	ms
	ダミーパルス幅	Tvdpw	770	μs
Hsync	遅延時間	Thd	1.4	μs
	サイクル時間	Thc	190	μs
	ダミーパルス幅	Thdpw	35	μs
Pclk	遅延時間	Tpd	65	ns
	サイクル時間	Tpc	66	ns
	パルス幅	Tppw	33	ns
	各ブロック間の遅延時間	Tpdb	200	ns
Data1-12	遅延時間	Tdd	34	ns
	サイクル時間	Tdc	66	ns

2 × 2 モード (Typ.)

項目		記号	定格値	単位
Vsync	遅延時間 (外部トリガモードのみ)	Tvd	390	μs
	サイクル時間	Tvc	230	ms
	ダミーパルス幅	Tvdpw	770	μs
Hsync	遅延時間	Thd	1.4	μs
	サイクル時間	Thc	190	μs
	ダミーパルス幅	Thdpw	110	μs
Pclk	遅延時間	Tpd	65	ns
	サイクル時間	Tpc	66	ns
	パルス幅	Tppw	33	ns
	各ブロック間の遅延時間	Tpdb	200	ns
Data1-12	遅延時間	Tdd	34	ns
	サイクル時間	Tdc	66	ns

4 × 4 モード (Typ.)

項目		記号	定格値	単位
Vsync	遅延時間 (外部トリガモードのみ)	Tvd	390	μs
	サイクル時間	Tvc	117	ms
	ダミーパルス幅	Tvdpw	770	μs
Hsync	遅延時間	Thd	1.4	μs
	サイクル時間	Thc	190	μs
	ダミーパルス幅	Thdpw	150	μs
Pclk	遅延時間	Tpd	65	ns
	サイクル時間	Tpc	66	ns
	パルス幅	Tppw	33	ns
	各ブロック間の遅延時間	Tpdb	200	ns
Data1-12	遅延時間	Tdd	34	ns
	サイクル時間	Tdc	66	ns

注) 有効数字 2 桁 (Tvc は除く。)

■仕様 (機能)

項目	C7942	C7943
読み出し回路	チャージアンプアレイ	
各アンプのフィードバック容量	0.15 pF	0.6 pF
ビデオ出力 (Data 1 - 12)	RS-422 (差動)12 ビット	
出力データレート	15.15 MHz	
同期信号 (Vsync, Hsync, Pclk)	RS-422 (差動)	
bin0, 1, ExtTrg, IntExt	TTL	

■ 絶対最大定格 (Ta=25 °C)

項目	記号	定格値	単位
デジタル回路供給電圧(+5 V)	D.vdd	+6.0	V
アナログ回路供給電圧(+5 V)	A.vdd	+6.0	V
アナログ回路供給電圧(±7.5 V)	V(+/-7.5)	±12	V
動作温度 (結露なきこと)	Topr	0 to +35	°C
保存温度 (結露なきこと)	Tstg	0 to +50	°C

■ 仕様 (指定のない場合は Typ. Ta=25 °C A.vdd= 5.0 V, D.vdd= 5.0 V, V (±7.5)= ±7.5 V)

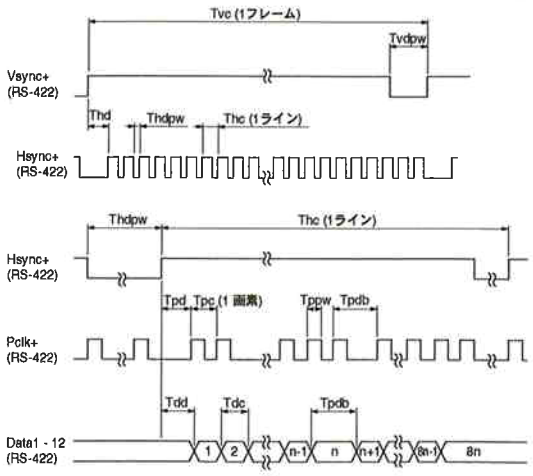
項目	記号	C7942	C7943	単位
画素サイズ	-	50	100	μm
受光面サイズ	-	120 × 120	124.8 × 124.8	mm
画素数	-	576 (2400 × 2400)	156 (1248 × 1248)	万画素
有効画素数 (水平 × 垂直)	-	2240 × 2368	1216 × 1232	画素
フレーム速度 (シングル動作)	Sf (int)	2	7	フレーム/s
フレーム速度 (2 × 2 ビニング)	-	4	15	フレーム/s
フレーム速度 (4 × 4 ビニング)	-	9	30	フレーム/s
外部フレーム速度 (シングル動作)	Sf (ext)	Sf (int) to 0.1	Sf (int) to 0.1	フレーム/s
雑音 (rms.)	N (rms.)	1100	2300	electrons
飽和電荷	Csat	2.2	10	M electrons
解像度	Reso	8	5	line pairs/mm
ダイナミックレンジ	-	2000	4300	-
欠陥ライン *	-	20 Max.	10 Max.	lines
シンチレータ	-	CsI		-

* 欠陥ライン: 感度=0 のライン。垂直・水平ともに、連続した欠陥ラインがないこと。

■タイミングチャート

フレームグラバボードで画像を得るには、以下を参考にしてソフトウェアのプログラム内またはパラメータファイル内にパラメータを記述してください。

内部モード



C7942: n=300
C7943: n=156

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■ その他の必要なシステム

C7942, C7943 の性能を十分に引き出して動作させるには、以下のシステムおよび周辺機器が必要です。
パソコン: Windows 98 以上で動く IBM-PC 互換機 (DOS/V マシン)
デジタルフレームグラバカード: モノクロ 16 ビット以上、ピクセルクロック 16 MHz 以上、同期信号 RS-422 インターフェース

ご使用になるグラバのマニュアルを参照してください。C7942, C7943 から 12 ビットのデジタル画像を取得する場合、ナショナルインストルメンツ社の IMAQ PCI-1424 (NI parts No. 777662-01)+増設メモリ 64 MB (NI parts No. 920130-64)で動作することが確認されています。IMAQ PCI-1422 (NI parts No. 777959-01)でも C7943 から画像を取得することが可能です。シンプルビュワとしてグラバに付属しているデモ用ソフトウエアで画像を取得し保存することができます。この場合, デモ用ソフトウエアのカメラ情報ファイルの使い方はユーザーズガイドに記されています。
電源: A.vdd=+5 V (700 mA), D.vdd=+5V (1000 mA), V (±7.5)=+7.5V (±100 mA)。電圧範囲は、A.vdd と D.vdd は 4.90 V～5.10 V、V (±7.5)は ±7.0 V～ ±8.0 V です。シリーズ電源を使用することをお勧めします (スイッチング電源の使用は避けてください)。
なお、C7942, C7943 用の電源ケーブル (片端が FGG.2B.307.CLAD92Z プラグ、他端が開放、長さ: 2 m、表 2 参照)は本体に付属しています。同期信号、ビデオ出力、外部コントロール信号用の 36 ピンケーブル (表 1 参照)はオプションで用意されています。
上記電圧範囲は、フラットパネルセンサ側での電圧です。付属の電源ケーブルは充分インピーダンスの低いものですが、ケーブル部で 0.1 V 程度電圧降下が生じます。電源側での電圧は 0.1 V 高めに設定してください。

表 1 36 ピンレセプタクルのピン接続

ピン No.	信号	ピン No.	信号
1	Data1+ (MSB)	19	Data1- (MSB)
2	Data2+	20	Data2-
3	Data3+	21	Data3-
4	Data4+	22	Data4-
5	Data5+	23	Data5-
6	Data6+	24	Data6-
7	Data7+	25	Data7-
8	Data8+	26	Data8-
9	Data9+	27	Data9-
10	Data10+	28	Data10-
11	Data11+	29	Data11-
12	Data12+ (LSB)	30	Data12- (LSB)
13	bin0 (TTL)	31	Gnd
14	bin1 (TTL)	32	Gnd
15	ExtTrg (TTL)	33	IntExt (TTL)
16	Vsync+	34	Vsync-
17	Hsync+	35	Hsync-
18	Pclk+	36	Pclk-

指定のない場合は、信号レベルは RS-422。
36 ピンプラグ TX20A-36PH1-D2P1-D1: 日本航空電子工業 (株)社の製品
36 ピンレセプタクル: TX20A-36R-D2GF1-A1L

表 2 電源ピン接続とケーブル色

ピン No.	色	信号
1	茶	+7.5 V
2	赤	アナログ GND
3	オレンジ	-7.5 V
4	黄	アナログ GND
5	緑	アナログ+5 V
6	青	デジタル GND
7	紫	デジタル+5 V
シールド	-	アナログ GND

7 ピン電源プラグ: FGG.2B.307.CLAD92Z は LEMO S.A.社の製品
7 ピン電源レセプタクル: ECG.2B.307.CLV

36 ピンケーブル (オプション)

A タイプケーブル: 汎用デジタルフレームグラバ用インターフェースケーブルです。
B タイプケーブル: IMAQ PCI-1424 グラバボード用インターフェースケーブルです。

タイプ	ケーブル型名	ケーブル長	ケーブル終端	ケーブル終端
A	A8406-01	5 m	TX20A-36PH1-D2P1-D1	オープン
	A8406-06	7 m		
	A8406-07	10 m		
	A8406-08	12 m		
B	A8406-02	5 m		PCS-XE100MA
	A8406-03	7 m		
	A8406-04	10 m		
	A8406-05	12 m		

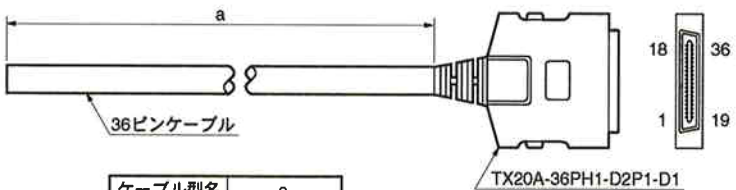
汎用フレームグラバ用ケーブル A8406-01/-06/-07/-08

A8406-01/-06/-07/-08 は、汎用フレームグラバとフラットパネルセンサ C7942, C7943 を接続するためのケーブルです。本ケーブルの片端には C7942, C7943 のデジタル出力用 36 ピンプラグが付いています。他端は開放ですので、ご使用になるデジタルフレームグラバに適合するプラグを接続してください。ケーブルの色仕様を下表に示します。

■ オープンケーブル色仕様

ピンNo.	信号	ケーブル色	マーク色	ピンNo.	信号	ケーブル色	マーク色
1	Data1+ (MSB)	青	-	19	Data1- (MSB)	オレンジ	-
2	Data2+	緑	-	20	Data2-	茶	-
3	Data3+	グレー	-	21	Data3-	赤	-
4	Data4+	黒	-	22	Data4-	黄	-
5	Data5+	ピンク	-	23	Data5-	紫	-
6	Data6+	白	-	24	Data6-	青	赤
7	Data7+	オレンジ	白	25	Data7-	緑	白
8	Data8+	茶	白	26	Data8-	グレー	白
9	Data9+	赤	白	27	Data9-	黒	白
10	Data10+	黄	黒	28	Data10-	ピンク	黒
11	Data11+	紫	白	29	Data11-	白	青
12	Data12+ (LSB)	青	赤	30	Data12- (LSB)	オレンジ	白
13	bin0 (TTL)	緑	白	31	Gnd	茶	白
14	bin1 (TTL)	グレー	白	32	Gnd	赤	白
15	ExtTrg (TTL)	黒	白	33	IntExt (TTL)	黄	黒
16	Vsync+	ピンク	黒	34	Vsync-	紫	白
17	Hsync+	白	青	35	Hsync-	青	黒
18	Pclk+	オレンジ	黒	36	Pclk-	緑	黒

■ 外形寸法図 (単位: mm)



ケーブル型名	a
A8406-01	5000 ± 140
A8406-06	7000 ± 140
A8406-07	10000 ± 140
A8406-08	12000 ± 140

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